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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,154	01/30/2002	Gayvin E. Stong	10011031-1	7570

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,154	STONG, GAYVIN E.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-18* is/are allowed.

6)☒ Claim(s) *1,4-10 and 19-24* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

An Amendment filed on 4-19-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 6-10 and 19-24 are rejected under 35 U.S.C. 102(b) as being anticipated by the Gujral et al reference (U.S. Patent 5,896,052).

Gujral discloses in figure 3 an apparatus comprising a plurality of flip-flops (3-1, 3-2, 3-01, 3-02, 3-03), each flip-flop capable of sampling data (D terminal) and outputting data only on an edge of a clock (operation of flip-flop), wherein the apparatus synchronizes data received by the synchronizer from first clock domain logic (IN block) at a first clock frequency (INPUT_CLOCK) to a second clock domain logic (OUT block) at a second clock frequency (OUTPUT_CLOCK), the first clock domain logic being controlled by a first clock that generates the first clock frequency, the second clock domain logic being controlled by a second clock that generates the second clock frequency second clock that generates the second clock frequency, the first and second clocks being synchronized to each other at regular intervals and having edges that coincide at the regular intervals (col. 2 and 3, lines 63-67, 5-9 and 55-59) the synchronizer having a Data In (INPUT) input and a Data Out (OUTPUT S-00) output and wherein logic gates of the first clock domain logic that are in a signal path (output of 3-1) that is

coupled to the Data In input are controlled in part in response to coincidences of the edges at the regular intervals to thereby provide the logic gates with a first clock cycle as a setup time margin (i.e., F-F 3-1 is triggered by the first clock) as required by claim 1.

As to claim 4, Gujral discloses the synchronizer providing logic gates of the second clock domain logic that are in a signal path that is coupled to the Data Out output of the synchronizer with a second clock cycle as a setup time margin (i.e., F-Fs 3-01 to 02 are triggered by the second clock).

As to claim 6, the functional recitation of this claim is considered to be inherent in Gujral because no additional element(s) of Applicant's synchronizer has been set forth in claim 6 (i.e., if there are additional elements in Applicant's invention which provides the recited function of claim 6, these additional element(s) must be put in claim in order to distinguish over the Gujral reference.

As to claim 7, col. 2, lines 63-67, discloses the frequency of the first clock (OUTPUT_CLOCK) is higher than that of the second clock. It is noted that signal (OUTPUT_CLOCK) can be interpreted as either the first clock or the second clock since the recitation of parent claim (i.e., claim 1) only calls for each domain having its own clock.

As to claim 8, col. 2, lines 63-67, discloses the frequency of the second clock (OUTPUT_CLOCK) is higher than that of the first clock.

As to claim 9, col. 2, lines 63-67 also discloses the ratio of the first clock frequency (OUTPUT_CLOCK) to the second clock frequency is 2-to-1. It is noted that signal (OUTPUT_CLOCK) can be interpreted as either the first clock or the second clock since the recitation of parent claim (i.e., claim 1) only calls for each domain having its own clock.

As to claim 10, col. 2, lines 63-67 also discloses the ratio of the second clock frequency (OUTPUT_CLOCK) to the first clock frequency is 2-to-1.

As to claim 19, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that figure 3 discloses a first input flip-flop 3-2 responsive to the first clock and an output flip-flop 3-02 responsive to the second clock.

As to claim 20, it is rejected for reciting a method/step derived from the rejected configuration claimed in claim 19.

As to claims 21 and 22, the scopes of claim are similar to that of claim 1. Therefore, they are rejected for the same reasons set for above. It is noted that col. 2, lines 63-33, discloses the ratio between input and output clocks is depends upon the minimum interval between input pulses (i.e., $f1 \geq (2/n)f2$ wherein n is an integer). Therefore, the ratio must be a non-integer for n=3.

As to claim 23-24, they are rejected for reciting a method/step derived from the rejected configuration claimed in claim 21.

Response to Arguments

3. Applicant's arguments filed 4-19-05 have been fully considered but they are not persuasive.

Applicant has argued that the two clocks of Gujral et al are asynchronous wherein the two clocks recited in claims are synchronous such that an edge of the first clock coincides with an edge of the second clock. Examiner respectfully disagrees with Applicant's position since in various places in BACKGROUND and DETAILED DESCRIPTION sections (i.e., col. 1, lines

15-17; 27-31, col. 3, lines 7-9; 55-59) Gujral's teachings imply that his circuit works well with both synchronous and asynchronous signals. In fact, col. 4, lines 5-9, indicates that a clock in one domain is synchronized to a clock in a different domain.

Allowable Subject Matter

4. Claims 11-18 are allowed.

5. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claim. Specifically, none of the prior art teaches or fairly suggests, among other things, the limitation *"Data Out output logic that receives the ordered data from the synchronization logic in said predetermined order and outputs the ordered data from the synchronizer to the second clock domain logic at the second clock frequency, wherein the Data Out output logic includes an output flip flop that receives and samples the ordered data and that outputs the data sampled thereby at said second clock frequency when an edge of said second clock is received by said output flip flop"* as recited in claim 2; and the limitation "*output logic that receives data values output from said synchronization logic and outputs data therefrom at the second clock frequency into the second clock domain, the output logic comprising at least one output flip flop that samples data on an edge of said second clock and that outputs the data sampled by the second flip flop on an edge of said second clock*" as recited in claim 11.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
5-20-05

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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